REMARKS

Claims 68-82, and 96-97 are pending in the application. Favorable reconsideration of the application is requested.

Withdrawal of the rejection of claim 76 under 35 U.S.C. § 112 is requested. The claim has been amended to avoid the concerns raised in the Office Action.

Applicants respectfully traverse the rejection to claim 68. The second insulating film in the second embodiment of the present application has a portion extending into the peripheral region as shown in FIGS. 3A and 3B. Thus, the specification, particularly the text supporting FIGS. 3A and 3B discloses on page 19, first full paragraph thereof that the second insulating film, the ono film, is disposed in the region where the peripheral transistor is formed as well as in the region of the memory transistor. Lines 13 and 14 recite the fact that the element isolation region is not covered by the second insulating film. The drawing figures, particularly FIGS. 1E, 1F, 1G and 1H demonstrate that the element isolation region is not covered by the second insulating film 6. Accordingly, it is believed that claim 68 is supported in the application.

Withdrawal of the rejection of claims 75, 79, 81 and 72 under 35 U.S.C. § 102 as being clearly anticipated by Usami et al. (U.S. Pat. No. 4,597,159) is requested. The Usami et al. (U.S. Pat. No. 4,597,159) reference discloses manufacturing a semiconducting device which includes only a memory transistor. In reviewing the reference, there is no second, peripheral transistor as is provided for in the method represented by the rejected claims. Further, the present application calls for a step of depositing a second insulating film over a first conductive film. A second conductive film overlies the second insulating film and an impurity is introduced into the second conductive film, at an concentration higher than the impurity in the first conductive film. Claim 75 has been amended to indicate that the impurities introduced to the second conducting films do not penetrate through the second insulation layer.

The cited reference demonstrates the implantation of impurities through a second insulation film 25 into the polycrystalline silicon film 24 (see FIG. 3C) and description in col. 4,

lines 32+. The reference fails to show, as is set forth in the rejected claims, an insulation layer which maintains or stops the introduction of impurities into the first conductive film.

This feature of Applicants claims remains totally undisclosed in the cited reference. Further, the cited reference fails to disclose the formation of two transistors, a memory transistor and a peripheral transistor as is provided for by the present application.

Applicant's claims further require that the impurity introduced into the second conductive film have a higher concentration than the impurities introduced into the first conductive film. In the example shown in the reference, the second film has a concentration within a range $4x10^{20}$ atoms/cm^3 to $6x10^{20}$ atoms/cm^3, which is lower than the impurity introduced into the first film ($5x10^{20}$ and $7x10^{20}$ atoms/cm^3). Accordingly, the reference is distinguishable from the claims in the application on this basis as well.

Withdrawal of the rejection of claims 68-71, 73, 74, 76-78 under 35 U.S.C. § 103 as being unpatentable over Usami et al. (U.S. Pat. No. 4,597,159) in view of Hisanobu et al. (JP 7-183411) is requested. As noted above, Usami et al. (U.S. Pat. No. 4,597,159) fails to disclose numerous elements of Applicants rejected claims. Further, as noted in the Office Action Usami et al. (U.S. Pat. No. 4,597,159) lacks the second insulating film comprising a multi layer film having an oxide film and a nitride film in a memory cell region but not in a peripheral region, and patterning the lamination of the second and first conductive layers in the peripheral circuit region. The reference as was noted above, fails to disclose any area for a peripheral circuit.

Hisanobu et al. (JP 7-183411) does disclose a peripheral transistor along with a memory transistor. The figures and translation (see copy enclosed) in the application show a memory transistor 13 and peripheral transistor 19 formed on the same substrate. The claimed method of the present application requires each of the conductive films to be doped with impurities, and that the second conductive films have a higher concentration of impurities than the first. It is not seen where any of the embodiments shown in this reference have any such impurities introduced into the conductive films. The use of the ono film to stop the higher concentration impurities from entering the first conductive film is also not disclosed in this reference.

The specification (see page 17, lines 10-17) makes clear that these process steps make it possible to have a low impurity concentration in the lower conductive film which preserves the tunnel oxide film while permitting the gate electrode resistance to be advantageously lowered.

The primary reference to Usami et al. (U.S. Pat. No. 4,597,159), also fails to disclose the relative concentration of impurities in the conductive films as claimed, i.e., the second conductive layer having a higher impurity concentration than the first conductive film. Accordingly, Usami et al. (U.S. Pat. No. 4,597,159) cannot be combined with the secondary reference to Hisanobu et al. (JP 7-183411) to show these process steps, or the benefits derived from this combination of process steps.

In view of the foregoing, it is not seen how the combination of the references can suggest a *prima facie* case of obviousness.

New independent claims 96 and 97 have been introduced into the application to claim the subject matter of previous claims 80 and 72 (now canceled) but which were deemed to contain allowable subject matter.

In view of the foregoing, favorable reconsideration is believed to be in order. In the event that the Examiner does not deem that this response place the application in condition for allowance, he is urged to contact the undersigned at the telephone number below. The undersigned respectfully requests that an interview be given in connection with this application to avoid any unnecessary appeal to the Board of Patent Appeals and Interferences.

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Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 22-0185, under Order No. 20433-00601-US1 from which the undersigned is authorized to draw.

Dated: 10/08/04

Respectfully submitted,

By _____

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